

## CLAIMS

What is claimed is:

- 1 1. A memory circuit, comprising:  
2 a first electrode formed on a support surface, the first electrode having a first  
3 electrode surface that intersects the support surface;  
4 a spacer positioned on the support surface adjacent to the first electrode surface;  
5 and  
6 a ferroelectric layer formed on the first electrode and the spacer.
- 1 2. The memory circuit of claim 1, further comprises a second electrode formed on  
2 the ferroelectric layer opposite of the first electrode.
- 1 3. The memory circuit of claim 1, wherein the spacer comprises of an insulation  
2 material.
- 1 4. The memory circuit of claim 1, wherein the ferroelectric layer comprises of a  
2 polymer.
- 1 5. The memory circuit of claim 1, wherein the support surface comprises of  
2 insulation material.
- 1 6. The memory circuit of claim 1, wherein a portion of the spacer nearest to the first  
2 electrode surface has a height about equal to a height of the first electrode, the height of  
3 the first electrode being a distance between the support surface and a second electrode  
4 surface of the first electrode, the second electrode surface being substantially parallel to  
5 the support surface.
- 1 7. The memory circuit of claim 1, wherein the spacer is in contact with the first  
2 electrode surface.

1 8. The memory circuit of claim 1, wherein the spacer is separated from the first  
2 electrode surface.

1 9. The memory circuit of claim 1, wherein the support surface is located on a die.

1 10. The memory circuit of claim 1, wherein the spacer is formed for a selected one of  
2 moving a transition point away from the first electrode, and reducing sharpness of a  
3 transition.

1 11. The memory circuit of claim 1, wherein the first electrode comprises first and  
2 second portions, the first portion comprising a first material that is non-reactive to the  
3 ferroelectric layer and located at a second electrode surface of the first electrode, the  
4 second electrode surface being parallel to the support surface, and the second portion  
5 comprising a second material that is more conductive than said first material and  
6 located between the first portion and the support surface.

1 12. The memory circuit of claim 11, wherein the spacer is formed against the first  
2 electrode surface such that the spacer isolates the second portion from the ferroelectric  
3 layer.

1 13. A method, comprising:  
2 forming a first electrode on a support surface, the first electrode having a first  
3 electrode surface that intersects the support surface;  
4 forming a spacer positioned on the support surface adjacent to the first electrode  
5 surface; and  
6 forming a ferroelectric layer on the first electrode and the spacer.

1 14. The method of claim 13, further comprises forming a second electrode on the  
2 ferroelectric layer opposite of the first electrode.

1 15. The method of claim 13, wherein said forming of a spacer comprises forming a  
2 portion of the spacer nearest to the first electrode surface with a height about equal to a  
3 height of the first electrode, the height of the first electrode being a distance between  
4 the support surface and a second electrode surface of the first electrode, and the  
5 second electrode surface being substantially parallel to the support surface.

1 16. The method of claim 13, wherein said forming of a spacer comprises forming the  
2 spacer by plasma enhanced chemical vapor deposition.

1 17. The method of claim 13, wherein said forming of a spacer comprises forming the  
2 spacer by depositing a spacer material on and around the first electrode and removing  
3 spacer material from a second electrode surface of the first electrode that is parallel to  
4 the support surface.

1 18. The method of claim 17, wherein the removing of the spacer material from the  
2 second electrode surface comprises removing the spacer material by a selected one of  
3 dry and wet etch.

1 19. The method of claim 13, wherein said forming of a spacer comprises forming the  
2 spacer for a selected one of moving a transition point away from the first electrode and  
3 reducing sharpness of a transition.

1 20. The method of claim 13, wherein said forming of a ferroelectric layer comprises  
2 forming the ferroelectric layer by spincoating.

1 21. A system, comprising:  
2 an integrated circuit, including  
3 a first electrode formed on a support surface, the first electrode having a  
4 first electrode surface that intersects the support surface,  
5 a spacer positioned on the support surface adjacent to the first electrode  
6 surface, and

7                   a ferroelectric layer formed on the first electrode and the spacer;  
8           a bus coupled to the integrated circuit; and  
9           a networking interface coupled to the bus.

1   22.   The system of claim 21, wherein the integrated circuit further comprises a second  
2   electrode formed on the ferroelectric layer opposite of the first electrode.

1   23.   The system of claim 21, wherein the spacer comprises an insulation material.

1   24.   The system of claim 21, wherein the ferroelectric layer comprises a polymer.

1   25.   The system of claim 21, wherein the support surface comprises an insulation  
2   material.